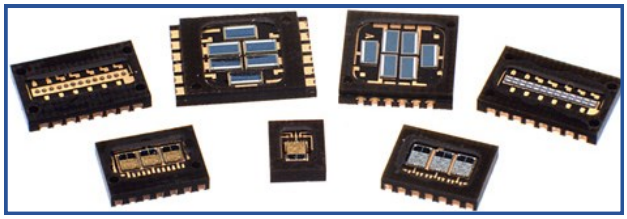
Surface Mount Chip Carriers (Hybrids)

Application Bulletin 240

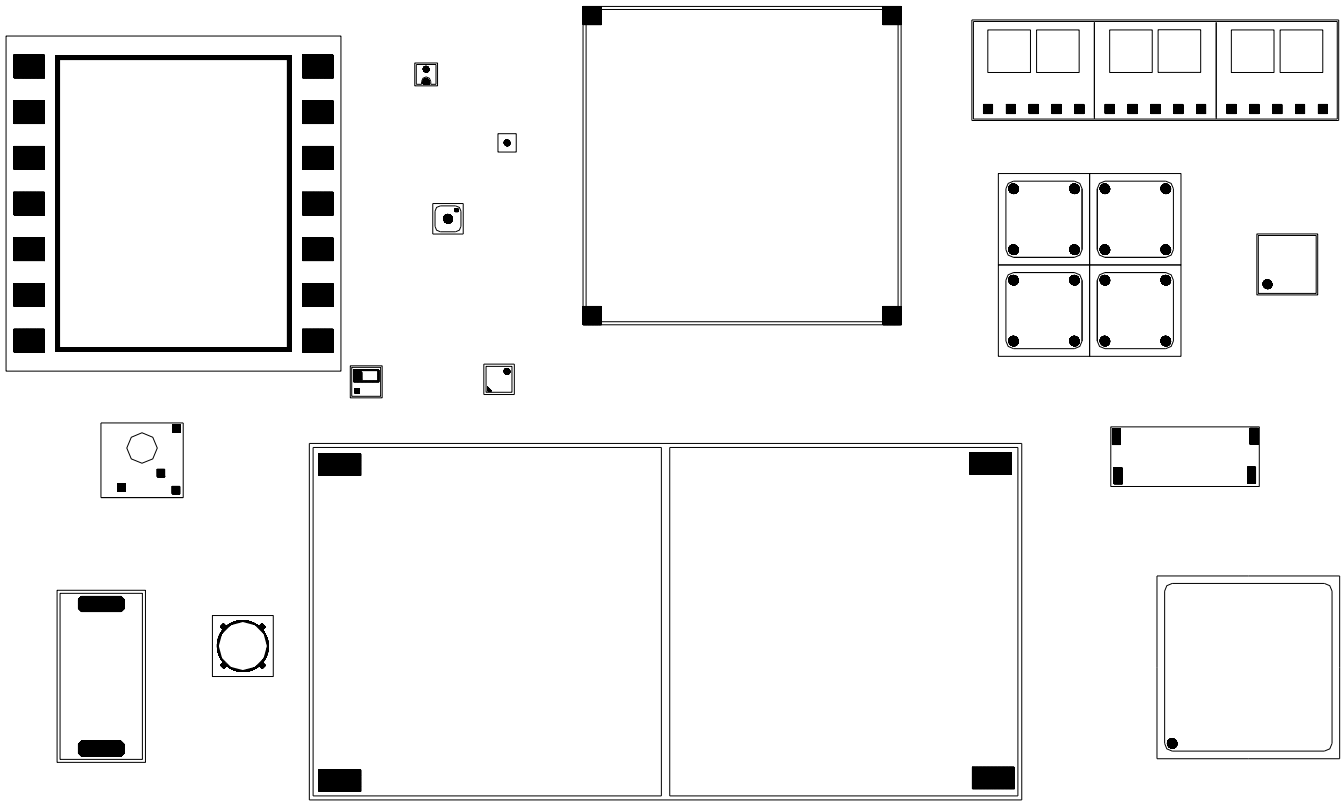
- Design Consideration



CUSTOM CAPABILITIES
Standard PC board fabrication flexibility allows for various component orientations, mounting features, and interconnect schemes.

The starting substrates can be epoxy-glass (FR4), polyimide, flex circuits, or ceramic. Production tooling is in place for a standard array format of 4" x 4", but custom tolling can be designed to meet the needs of other materials, sizes, and shapes.

Substrates, encapsulants, and plating can be tailored to meet the circuit requirements.



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Surface Mount Chip Carriers (Hybrids)

Even with the standard chip carrier materials and processes, imagination is the only limit to the possible configurations.

Design variables include:

- Materials
- Optical Properties
- Leads, Pins, or Cables
- Special Tests and Processing

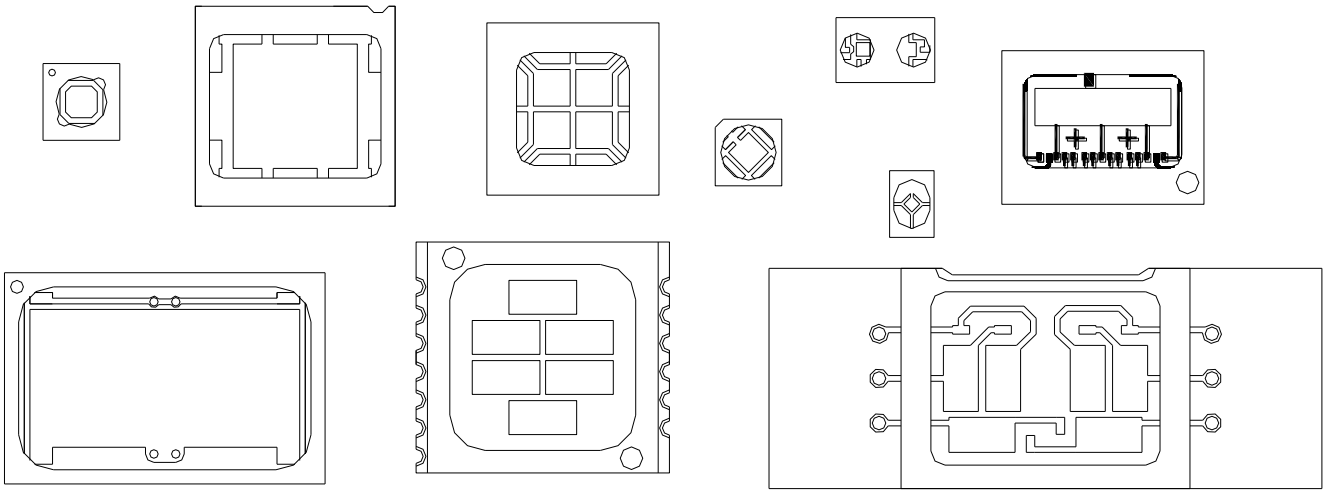
Optek produces a variety of IC's, photosensors, and light emitting diodes that can be incorporated in custom designs. Optek is not limited to the sensor applications which use optoelectronics. Starting at the chip level, we design, develop, and manufacture state-of-the-art Hall effect and power devices.

When standard devices are not a match, our internal design capability will satisfy the application circuit requirements.

Manufacturing flexibility makes the hybrid facility effective for serving both the high complexity and high volume assembly needs.

Computer controlled manufacturing operations include:

- Chip and SMD pick and place
- Wire bonding
- Encapsulant dispensing
- Singulating
- Cure and reflow oven cycles
- Final electrical test



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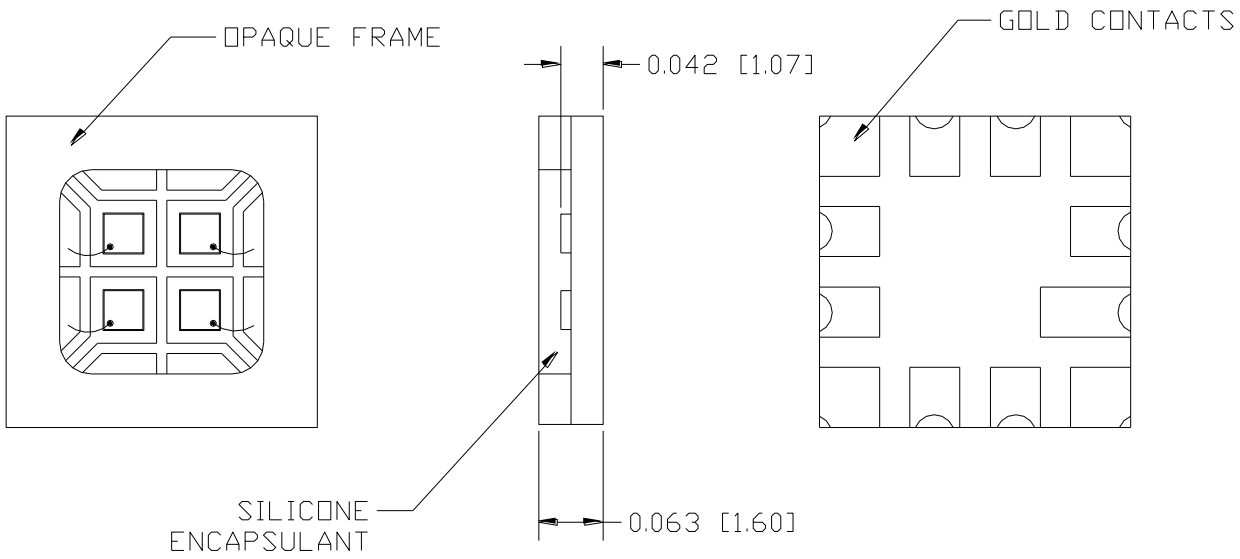
DESIGN RULES

The most cost effective chip-on-board products take advantage of standards in design and processing. The following guidelines for substrate layout are intended TO ASSIST the design in the first stage of product development.



The Chip Carrier

The FR4 chip carrier, an Optek standard packaging method, has four main parts: substrate, frame, components, and encapsulation. The substrate is fabricated from high temperature copper-clad laminate. Standard PC board processing provides the plated and non-plated holes, circuit patterns, and chip mounting features. The frame layer is made from the same polyimide laminates.

To make the substrate compatible with die attach and wire bonding techniques, the copper surface is plated with a nickel barrier and gold. After the chip components are mounted and bonded, the frame is screen printed with a pattern of non-conductive epoxy, aligned with the matching substrate cells and laminated under elevated temperature and pressure.

A conformal coating is applied to fill the component cavities. After curing, the array is sawed into individual product elements and ready for test.

The Substrate Material

The Optek standard chip carrier substrate and frame thickness is .028”. Including the adhesive and metal layers, this two layer, laminated package has a nominal thickness of .063”.

While thinner substrates can be specified (commercially available materials as thin as .005”), the standard thickness frame layer is ideal for encapsulants containment and insuring complete protection of the chips and bond wires.

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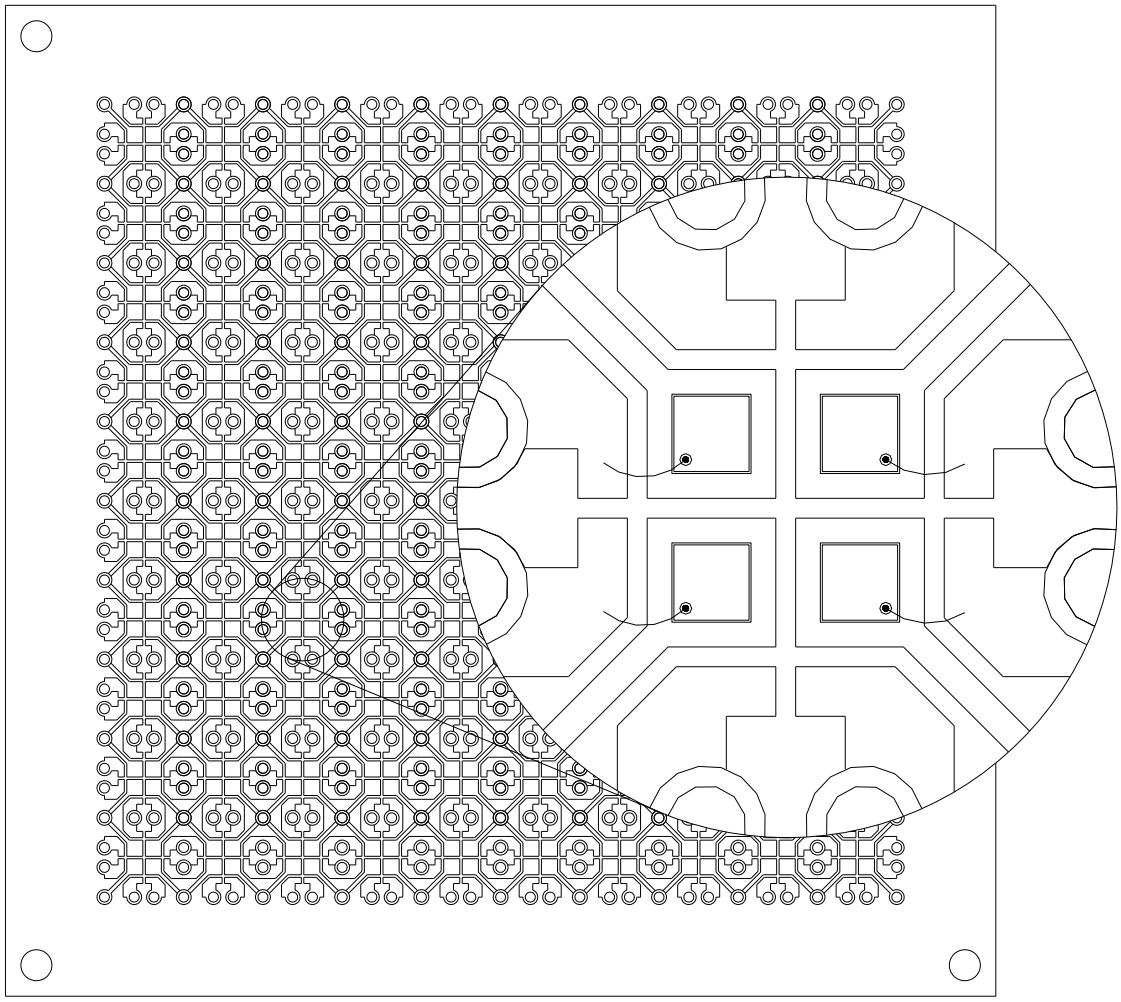
Surface Mount Chip Carriers (Hybrids)

The FR4 substrate used by Optek has a glass transition temperature (Tg) greater than 150°C. It is an excellent material because of its strength, processing temperature, and close match with the expansion coefficient of silicon devices. Also, it is commonly used in the surface mount industry. Where necessary, Optek also has available a special opaque grade of this material which can effectively shield sensors from stray light. The specifications and curves shown on the following page illustrate these characteristics.



Polyimide and other high temperature epoxy-glass laminates are also suitable for the chip-on-board processing and may be recommended for certain applications.

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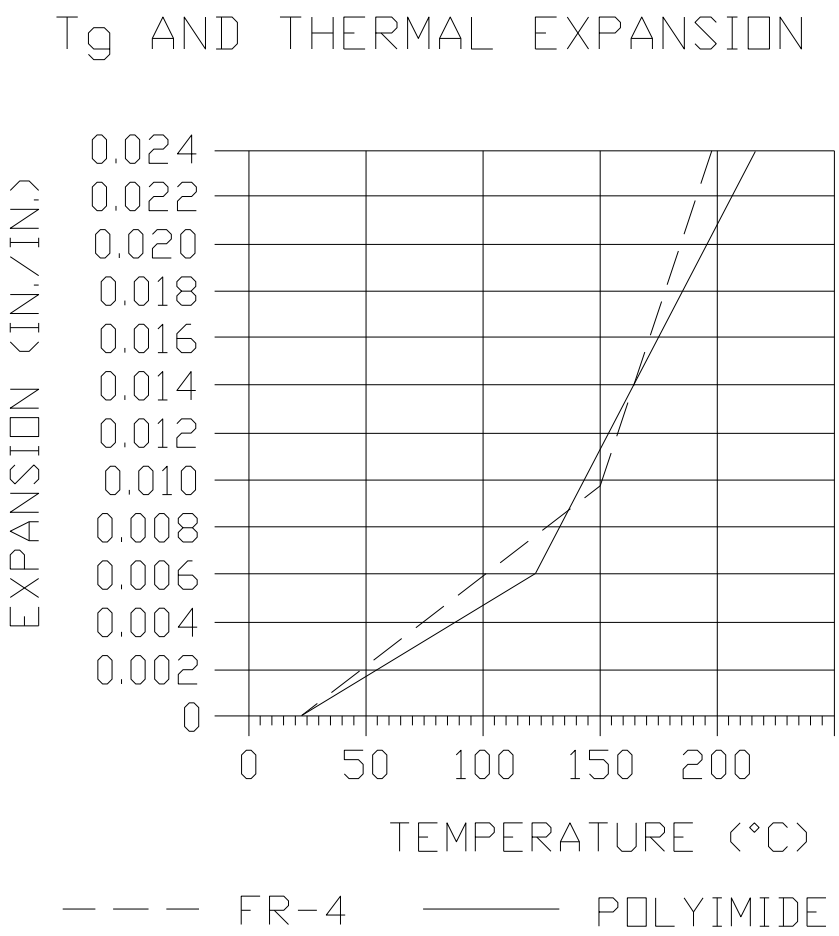
FR4, Tg>150°C, Substrate Characteristics

Operating Temperature (10k Hours)	145°C
Glass Transition Temperature (T_g)	150°C
Flammability (UL94)	V-0
Coefficient of Thermal Expansion (µin./in./°C)	Below T_g = 65 Above T_g = 300
Peel Strength (Pounds/Inch)	9
Flexural Strength (psi @ 200°C)	72,000
Water Absorption (%)	0.15
Dielectric Constant (@ 1 MHz)	4.6
Dissipation Factor (@ 1 MHz)	0.015
Volume Resistivity (Ohm-cm @ 25°C)	4.7×10^{14}
Surface Resistivity (Ohm @ 25°C)	5.3×10^{13}



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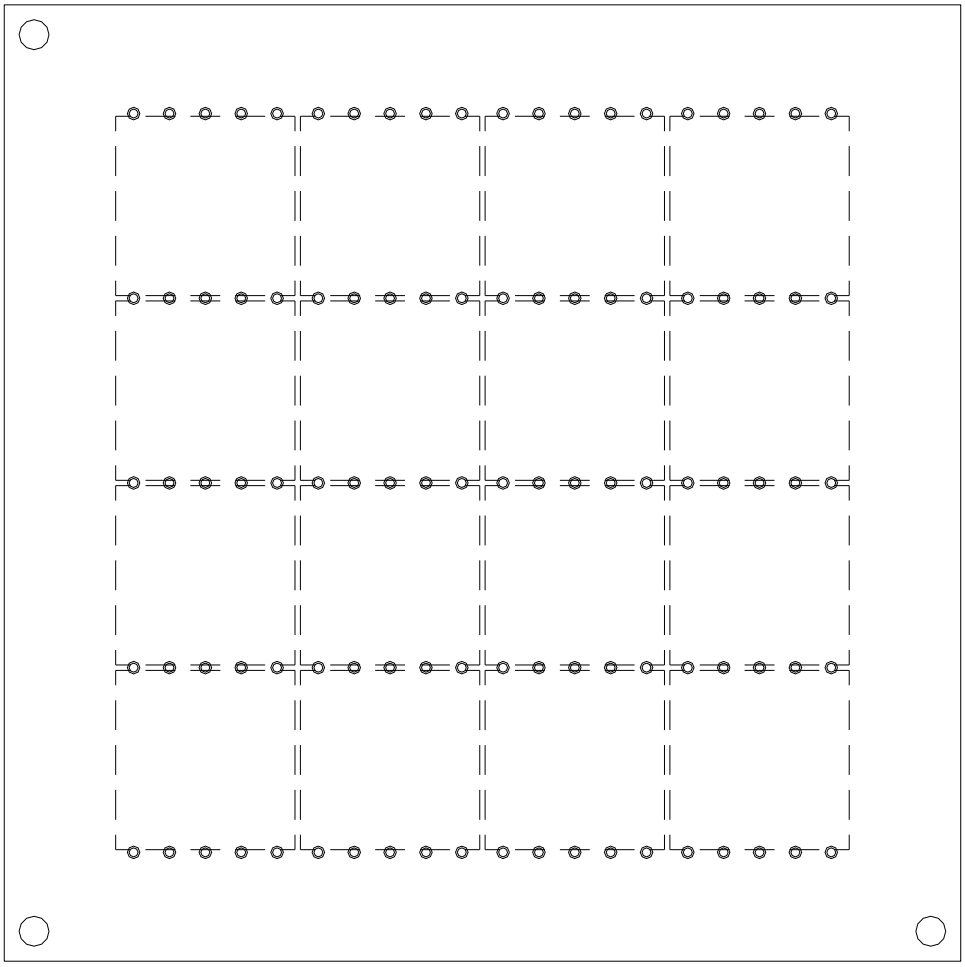
The Substrate Layout

Minimizing the size of the final package maximizes the cost effectiveness of the array process. As shown in the figure below, improved packing density is possible on the 4” x 4” substrate when cells are arranged to share through hole connections. A “half hole” contact remains with each cell when the elements are cut into the individual parts. Individual cells are arranged with separations or borders of .015”. This is the thickness of the standard saw blade used for separation. Wide blades are available to accommodate special perimeter features.



The Metal Pattern Features

Conductor widths and spaces of .015” are preferred where the design allows. Lines and spaces of less than .005” should be avoided for optimum pattern uniformity.

Conductor thickness is determined by the specified starting material and secondary plating process. Standard double-sided substrates have a minimum of 25 µin. of gold over 200 µin. of nickel over copper plating that is .0015” to .0020” thick. (Note that in areas where wire bonds are stitched, the gold plating is 30 µin. thick).

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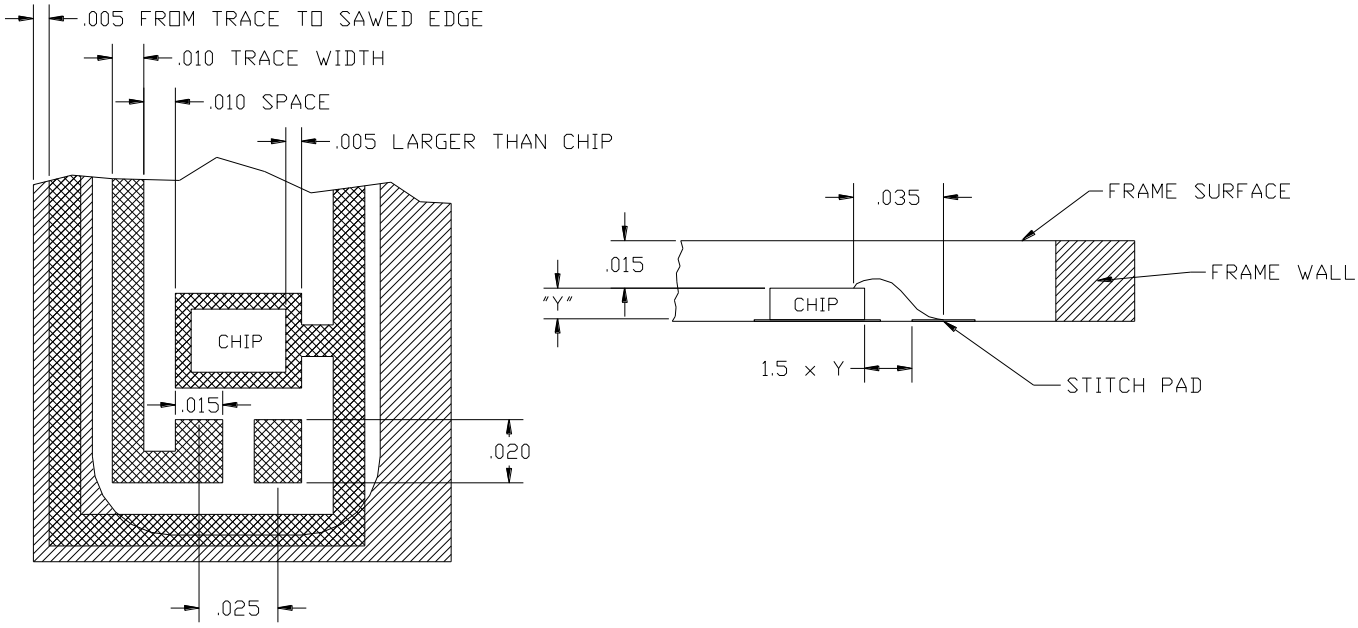
Alignment between the metal pattern and drilled or routed features is held to ±.003”. Chip registration may be specified in relation to substrate holes or the sawed perimeter to eliminate the metal to hole pattern tolerance as a consideration.

The wire bonding stitch pads on the metal pattern are nominally .015” x .020” with the longer dimension aligned with the bond wire. Stitch pads of .007” x .015” are considered the minimum size.

Stitch pad spacing (pad to pad) can be as close as .012”. Larger spacing (.020” is ideal) is always preferable for optimizing processing speed and inspection.



Chip mounting pads are often sized to be at least .005” larger than small chips such as LEDs. Even larger pads may be desirable for increased power dissipation or to provide a greater light reflecting surface. The mounting pad can be as small as the die itself for larger components. The pad edges can then be used as chip alignment features. This is particularly useful for designs where the metal pattern establishes a datum.

Drill, Rout, and Saw Features
For standard thickness substrates (.028”), hole diameters should be no smaller than .015”. Diameters of .008” have been used but should be avoided where possible and should be limited in number. Drilled holes of .020” or larger are used for most applications. Holes are guaranteed to be within ±.002” of absolute position.

When specifying .062” thickness for the substrate layer, the minimum recommended hole diameter is .030” to minimize cost.

To make leaded parts, square pins can be pressed into substrate holes. Standard press fit terminals (.025” square) require enough substrate area for a .031” diameter plated through hole with a pad diameter of .062”. Pin centers should be no closer than .050” to the perimeter of the part to avoid fracturing the laminate.

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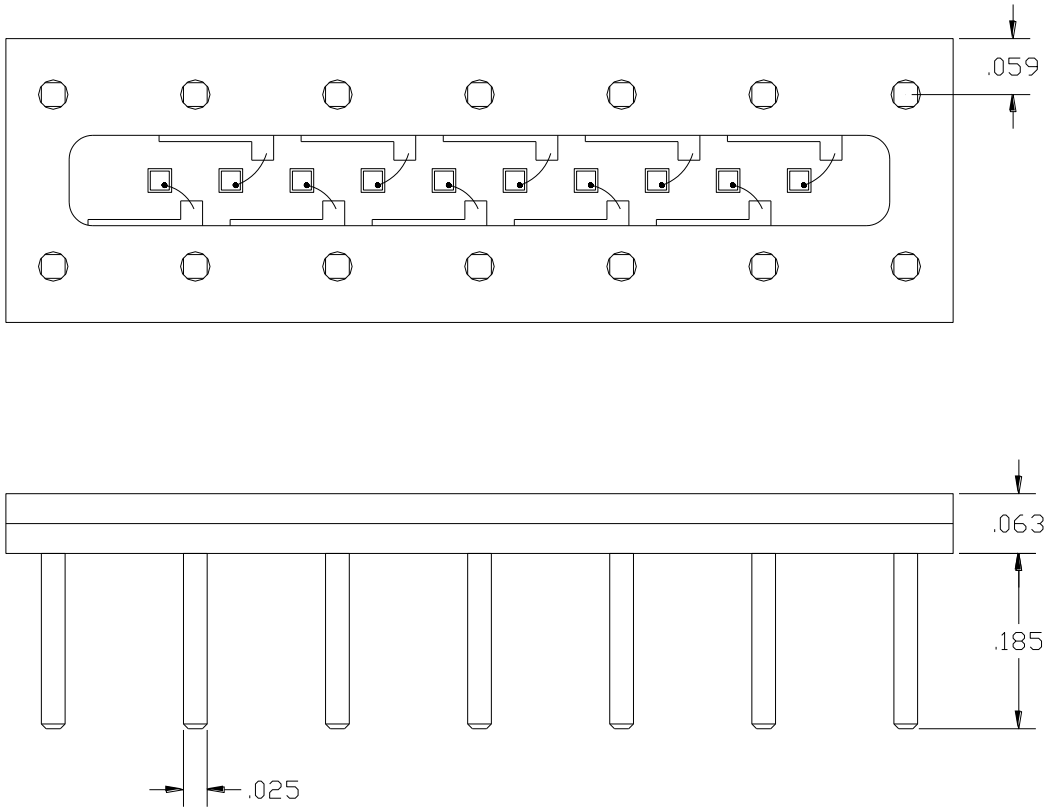

Wrap around edge contacts, formed by saw separation of plated through holes at cell boundaries, must be designed to accommodate the width of the blade. To insure a reliable contact remains after saw, the boundary holes shold be no smaller than .025". The half hole contacts can be made smaller only if they are offset from the boundary centers so that .005" minimum of the hole remains after saw.

The tolerance between drilled features and any of the sawed edges is held to within ±.005". Standard edge to edge tolerance is ±.005".

When sawed edges are specified in relationship to chip position, a total tolerance of ±.005" is used.

Wherever the design permits, metal patterns are typically recessed a minimum of .005" from these sawed edges to minimize metal flash or burrs between conductors.

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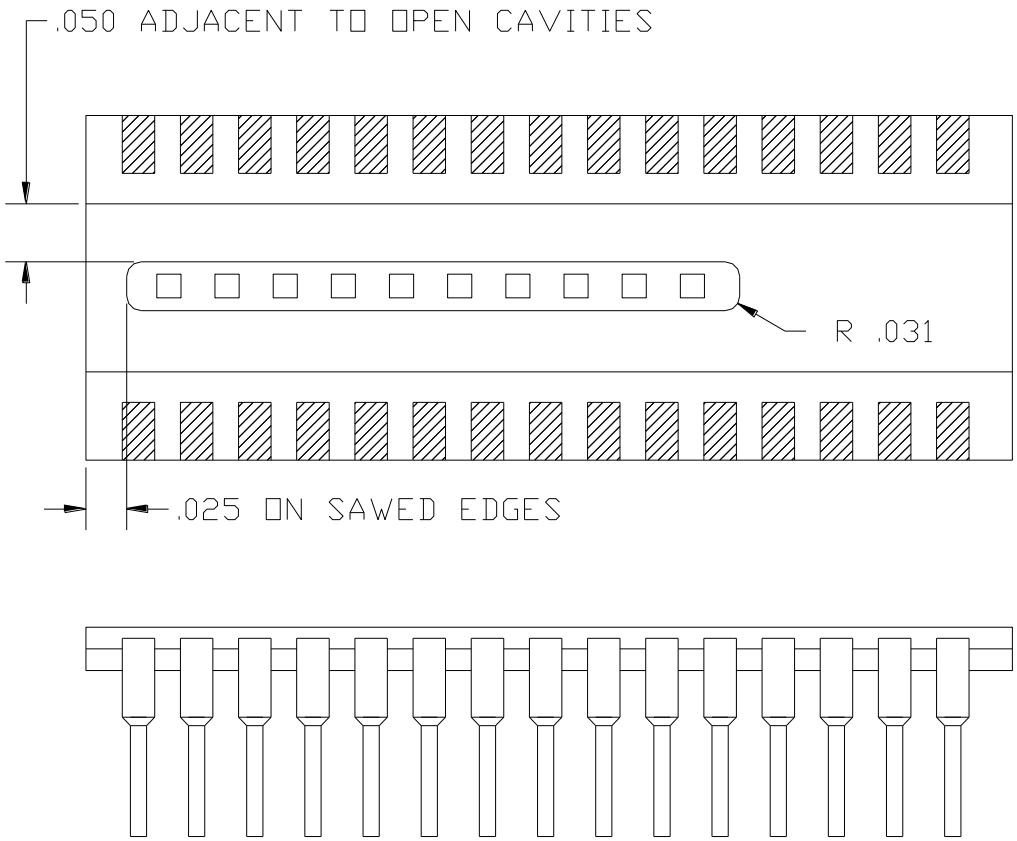
Frame Size and Shape

The size of the routed frame is often based on the need for including features for mounting or alignment with other components. Minimizing the size of a framed carrier depends on chip placement, the arrangement of wire bond patterns, and strength considerations.



The frame width (distance from the chip cavity to an outside edge) is recommended to be .050" when space allows. A wide frame insures maximum adhesion to the substrate and prevents low viscosity encapsulant from escaping the cavity. This is especially important for wall sections adjacent to unfilled cavities where a width of .040" should be considered the absolute minimum. Thinner walls are effective encapsulant barriers when adjacent cavities are also filled. Minimum wall width is also affected by the cavity size. Longer sections require wider walls for strength. Frame walls of .025" or wider are recommended.

The frame cavities can be a variety of shapes and sizes, but because they are formed by a routing operation, inside features are rounded. Chip placement must accommodate these radii which are nominally .031. The smallest radius which can be specified for standard processing is .025".

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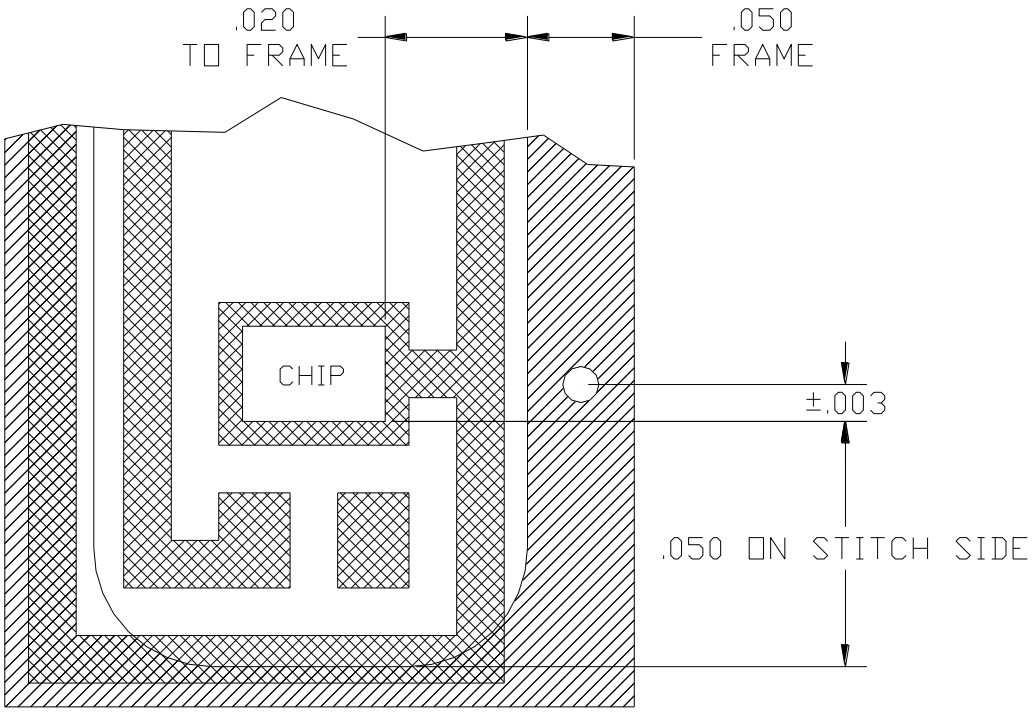
Chip Placement and Wire Bonds
Chip position may be specified with relation to drilled holes, routed or sawed edges, or the circuit's metal pattern. Registering the chips (especially sensors and LEDs) to holes is typically done when these holes will be used for aligning the carrier to features of the next level assembly or other optical components such as aperture masks.

Precise alignment marks can also be added to the metal patterns to produce a common datum for the die and carrier placement.

The relationship of the chip to the inside edge of the frame can vary greatly by the components selected (chip size and bond pad arrangement). In general, a chip edge can be as close as .015" to the frame where room is not required for bond wires. Spacing of .020" is preferred.



To allow room on a wire bonded side, the design rules call for .050" between the frame and the chip if possible and .035" as an absolute minimum.

The position of the bond pads on the chip is an important factor. A distance of .035" from the ball bond to the stitch bond is recommended when calculating the stitch pad position and the spacing to the edge of the frame. This allows for .015" nominal distance between the frame and stitch.

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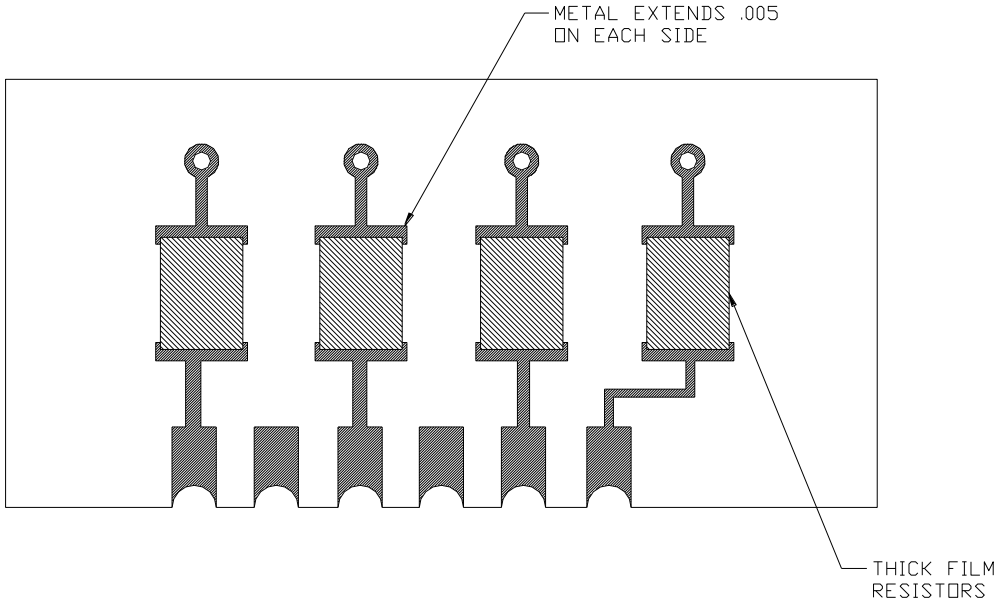
Screen Printed Materials

The alignment tolerance between the substrate and a screened image, such as solder mask, thick film resistors, or solder paste, is ±.005”. Metal pattern features are made slightly larger than the screened image to include this tolerance.

Special processes can improve this tolerance to ±.003” for some materials and geometries.



Polymer thick film resistor pastes range from 3 ohms per square to 1 Megaohm per square with a temperature coefficient of less than 100 ppm/°C.

Without laser trimming, the screened resistor typically has a value tolerance of 20%.

The resistor tolerance after trimming varies by the type and rate of the trimming performed and can be limited by the image size. Standard processing produces a trim tolerance of 1%, but wider tolerances enable faster trims and lower processing costs.

Design rules allow for trimmable resistors as small as .040” and untrimmed resistors as small as .020”.

Discrete components may be placed on the back side of the substrate along with screened materials. Most surface mount parts can be placed automatically. Pad size and spacing for such components should follow manufacturer recommendations.

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Encapsulation
The standard chip carrier construction is compatible with a wide variety of encapsulation materials, viscosities, and cure cycles because the framed cavities are completely enclosed and deep enough for any chip and bond wire profile.

Silicone is used as the standard encapsulation because of its wide operating temperature range, excellent adhesion, and ease of processing. It is ideal for optoelectronic applications because of its clarity and resistance to abrasion in subsequent cleaning operations.

Other encapsulants may be indicated where specific mechanical or chemical environments are not compatible with silicone. The material or its characteristics may be specified for new products.

The specifications for Optek's standard silicone are shown below.

Silicone Characteristics

Tensile Strength……500 PSI
Elongation……200%
Durometer, Shore A……30
Operating Temperature Range……-55°C to +200°C
Refractive Index @ 25°C…… 1.43
Linear Coefficient of Expansion (in./in./°C)……0.00021
Dielectric Constant @ 1 kHz……3.0
Dielectric Strength @ 1 kHz……500 V/mil
Sodium Ion Content……2 ppm
Potassium Ion Content……4 ppm

Temperature Limits of the Package
The operating temperature range of any particular design will typically be limited by the performance of the circuit components.

Special encapsulants and other attached components such as molded plastic lenses or housings must also be considered in both the operating and processing temperature of the chip carrier.

The standard silicone encapsulated polyimide package can withstand an environment of –55°C to +150°C indefinitely.

Reflow soldering of the surface mount packages can be performed with infrared, vapor phase, convection, or wave solder methods. The recommended limit for vapor phase reflow (up to 235°C) is 30 seconds. It is imperative that the MSL rating of the part (located on the packaging) be taken into consideration when soldering the part.

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