

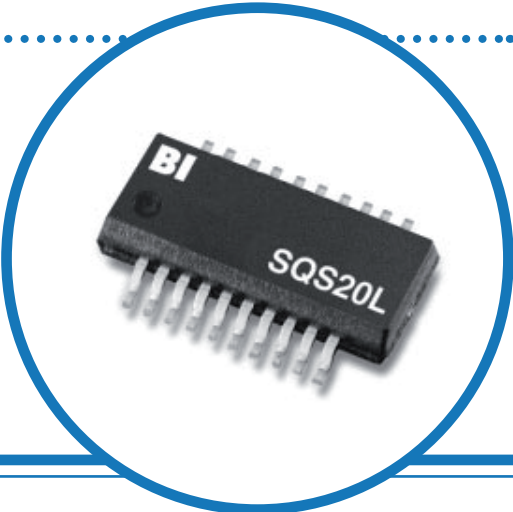
Nichrome Resistor Networks on Silicon Substrates



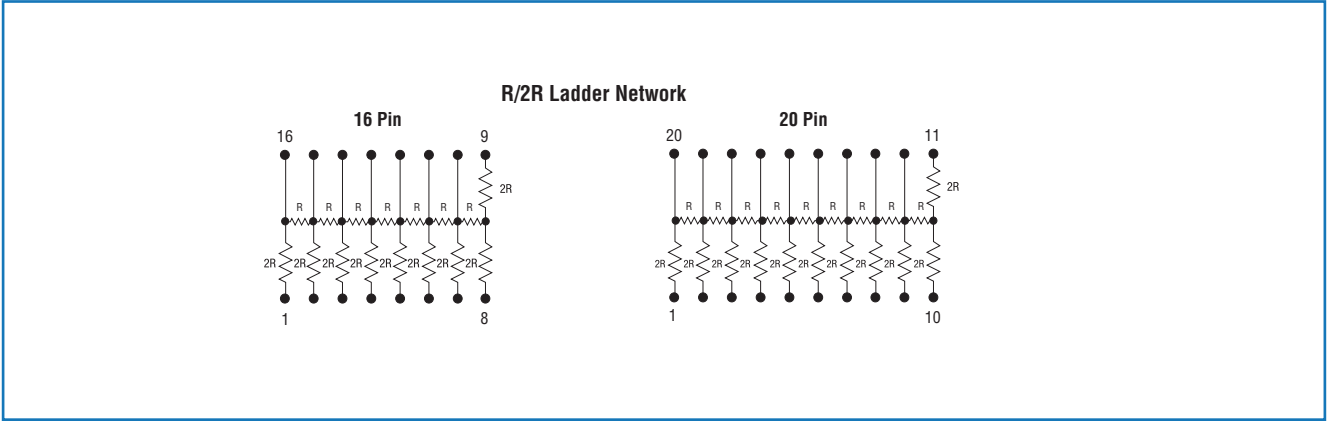
Models SQSxxL, SSNxxL, SSWxxL.

- Ladder Circuit
- Thin Film
- Resistor Networks
- RoHS Complaint
- Jedec 95 Industry standard packaging

OBSOLETE
Not Recommended for New Designs



Schematics



Electrical

Standard Resistance Range, Ohms	22 to 70K
Operating Temperature Range	-55°C to +125°C
Interlead Capacitance	<2pF
Insulation Resistance	≥10,000 Megohms
Noise, Maximum (MIL-STD-202, Method 308)	-25dB
Maximum Operating Voltage	100Vdc or \sqrt{PR}

Environmental (Mil-R-83401)

Thermal Shock plus Power Conditioning, Maximum	ΔR 0.1%
Moisture Resistance, Maximum	ΔR 0.1%
Mechanical Shock, Maximum	ΔR 0.1%
High Temperature Exposure, Maximum	ΔR 0.1%
Marking Permanency	per MIL-STD-202, Method 215
Flammability	UL-94V-O Rated
Storage Temperature Range	-55°C to +125°C

Specifications subject to change without notice.

General Note

TT electronics reserves the right to make changes in product specification without notice or liability.
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Mechanical

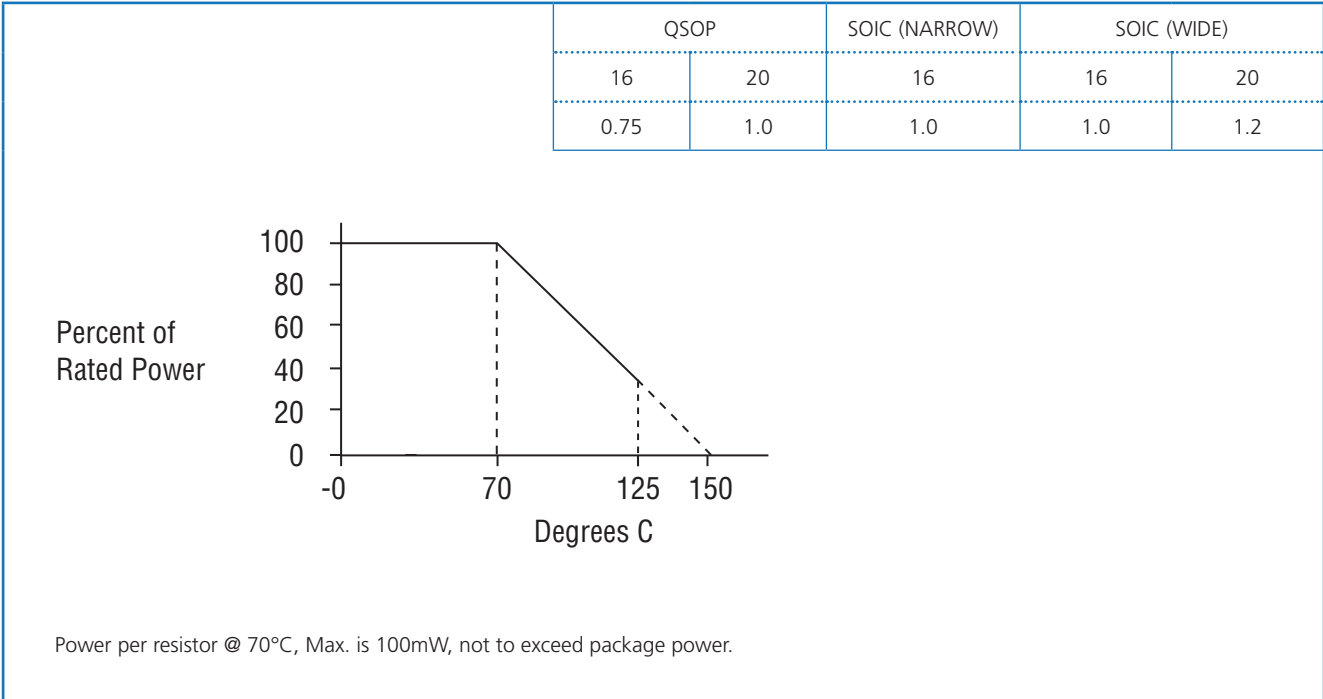
Lead Plating	100% matte Tin (RoHS)
Lead Material	Copper Alloy
Lead Configuration	Gull Wing
Lead Coplanarity	0.004" (0.102mm)
Substrate Material	Silicon
Resistor Material	Passivated Nichrome
Body Material	Molded Epoxy

Tolerances

Accuracy Code	F	G	J
Absolute Resistance Tolerances at 25°C	± 1.0%	± 2.0%	± 5.0%
Ratio Tolerances at 25°C	± 1.0%	N/A	N/A
Temperature Coefficient of Resistance (TCR Code)	±25ppm/°C (Q) ±50ppm/°C (P) ±100ppm/°C (S)		
Temperature Coefficient of Resistance, Tracking	±5ppm/°C		

Power Derating Curve

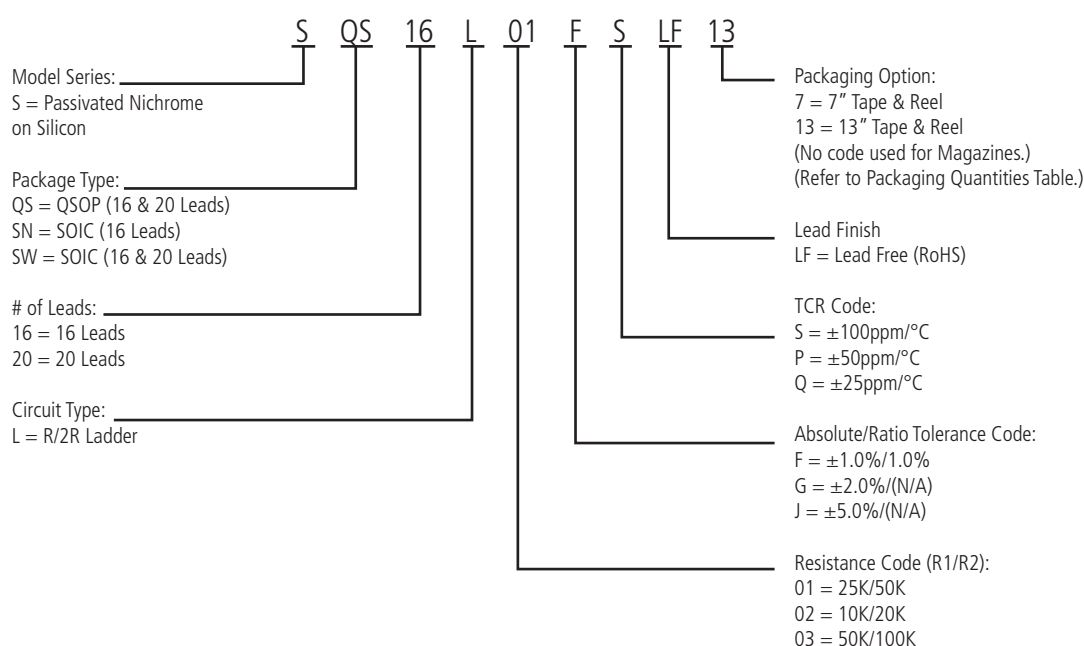
Package Power, Watts @ 70°C, Max.



Outline Dimensions

Package	Code	Lead Count	Mechanical Outline
QSOP	QS	16, 20	MO-137
SOIC Narrow Body	SN	16	MS-012
SOIC Wide Body	SW	16, 20	MS-013

Ordering Information



Custom Solutions

Networks designed to meet your specific electrical and packaging requirements are available. Please contact the factory for technical assistance, price and availability.

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