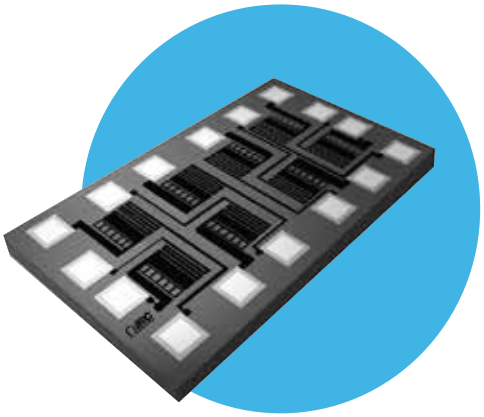
Resistors

OBSOLETE

Wire Bondable Resistor Network Arrays



Chip Network Array Series

- Absolute tolerances to ±0.1%
- Tight TCR tracking to ±5ppm/°C
- Ratio match tolerances to ±0.05%
- Ultra-stable tantalum nitride resistors

All parts are Pb-free and comply with EU Directive 2011/65/EU amended by (EU) 2015/863 (RoHS3)

IRC's TaNSil® network array resistors are ideally suited for applications that demand a small footprint. The small wire bondable chip package provides higher component density, lower resistor cost and high reliability.

The tantalum nitride film system on silicon provides precision tolerance, exceptional TCR tracking and low cost. Excellent performance in harsh, humid environments is a trademark of IRC's self-passivating TaNSil® resistor film.

For applications requiring high performance resistor networks in a low cost, wire bondable package, specify IRC network array die.

Electrical Data

		Isolated	Bussed
Resistance Range		10Ω to 2.5MΩ	10Ω to 1.25MΩ
Absolute Tolerance		to ±0.1%	
Ratio Tolerance to R1		to ±0.05%	to ±0.1%
Absolute TCR		to ±25ppm/°C	
Tracking TCR		to ±5ppm/°C	
Element Power Rating		100mW @ 70°C	50mW @ 70°C
Package Power Rating		8-Pad 400mW @ 70°C 16-Pad 800mW @ 70°C 24-Pad 1.0W @ 70°C	
Rated Operating Voltage (not to exceed $\sqrt{P \times R}$)		100V	
Operating Temperature		-55°C to +150°C	
Noise		<-30dB	
Substrate Material		Oxidized Silicon (10KÅ SiO_2 minimum)	
Substrate Thickness		0.016˝ ±0.001 (0.406mm ±0.01)	
Bond Pad Metallization	Aluminum	10KÅ minimum	
	Gold[1]	15KÅ minimum	
Backside		Silicon (gold available[1])	
Passivation		Silicon Dioxide or Silicon Nitride	

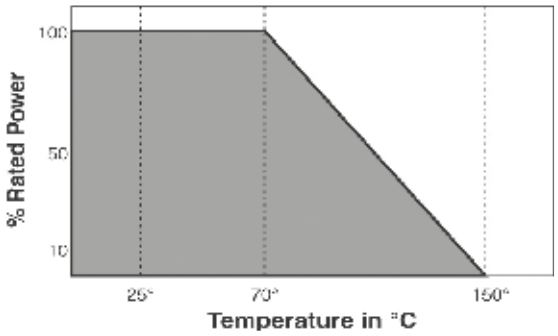
Note 1: Not recommended for new designs

TCR/Inspection Code Table

Absolute TCR	Commercial Code	MIL Inspection Code*
±300ppm/°C	00	04
±100ppm/°C	01	05
±50ppm/°C	02	06
±25ppm/°C	03	07

*Notes: Product supplied to Class H of MIL-PRF 38534 include 100% visual inspection

Power Derating Data



General Note

TT Electronics reserves the right to make changes in product specification without notice or liability.
All information is subject to TT Electronics' own data and is considered accurate at time of going to print.

BI Technologies IRC Welwyn

www.ttelectronics.com/resistors

Manufacturing Capabilities Data

Absolute TCR (±ppm/°C)	Isolated schematic A				Bussed schematic B			
	Ohmic range (Ω)	Available tolerances	Available ratio tolerances	Best TCR tracking (±ppm/°C)	Ohmic range (Ω)	Available tolerances	Available ratio tolerances	Best TCR tracking (±ppm/°C)
300	10 - 25	F G J	F G	50	10 - 25	F G J	F G	200
	26 - 50	D F G J	C D F	10	26 - 50	F G J	D F G	100
	51 - 200	C D F G J	C D F G	5	51 - 100	D F G J	C D F G	50
	201 - 2.5M	B C D F G J	A B C D F G	5	101 - 200	D F G J	B C D F G	25
					201 - 500	B C D F G J	B C D F G	20
					501 - 1.25M	B C D F G J	A B C D F G	5
100	26 - 50	D F G J	C D F G	10	26 - 50	F G J	D F G	100
	51 - 200	C D F G J	C D F G	5	51 - 100	D F G J	C D F G	50
	201 - 2.5M	B C D F G J	A B F G	5	101 - 200	D F G J	B C D F G	25
					201 - 500	B C D F G J	B C D F G	20
					501 - 350K	B C D F G J	A B C D F G	5
50	26 - 50	D F G J	C D F G	10	51 - 100	D F G J	C D F G	50
	51 - 200	C D F G J	C D F G	5	101 - 200	D F G J	B C D F G	25
	201 - 2.5M	B C D F G J	A B F G	5	201 - 500	B C D F G J	B C D F G	20
					501 - 1.25M	B C D F G J	A B C D F G	5
25	51 - 200	C D F G J	C D F G	5	201 - 500	B C D F G J	B C D F G	20
	201 - 2.5M	B C D F G J	A B F G	5	501 - 1.25M	B C D F G J	A B C D F G	5

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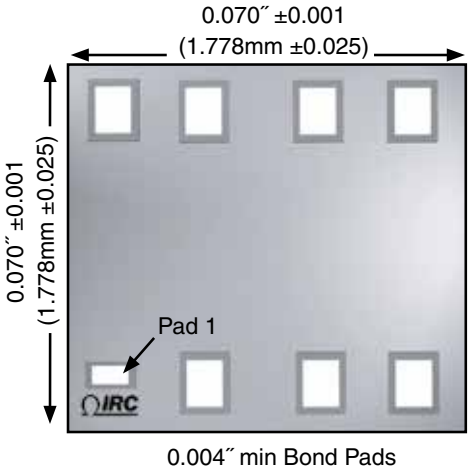
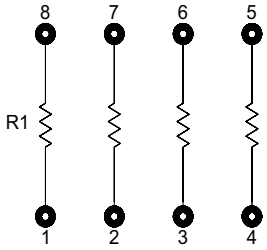
Chip Network Array Series

Physical Data

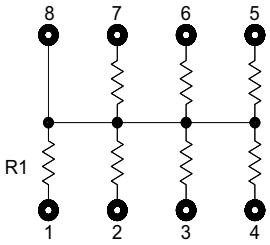
DSS4X



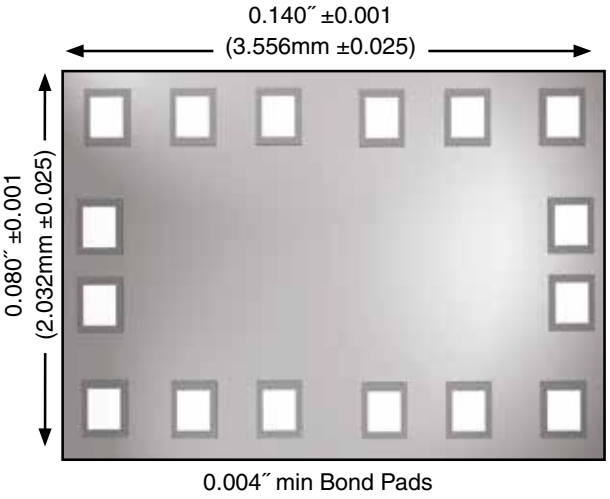
DSS4A



DSS4B



DSS8X



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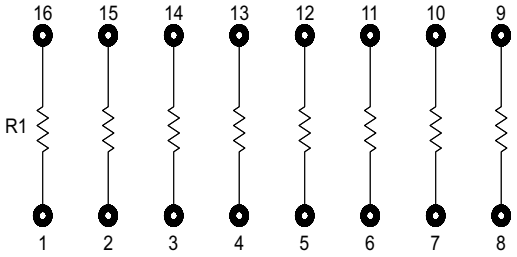

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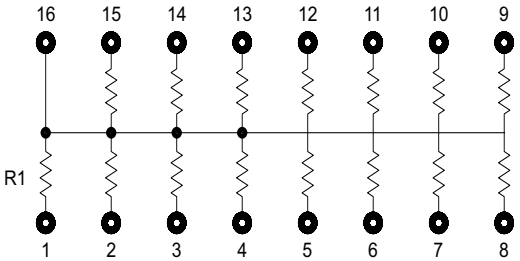

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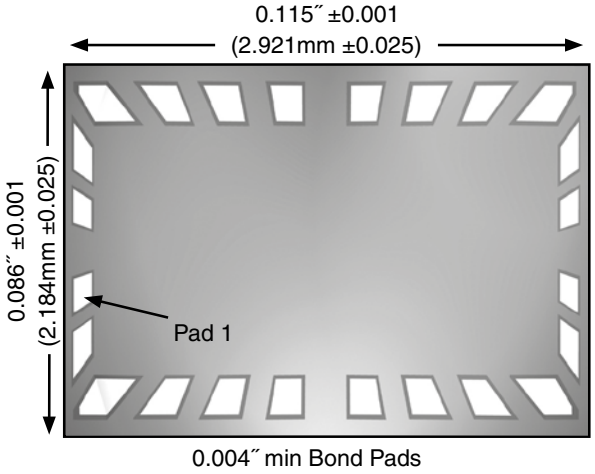
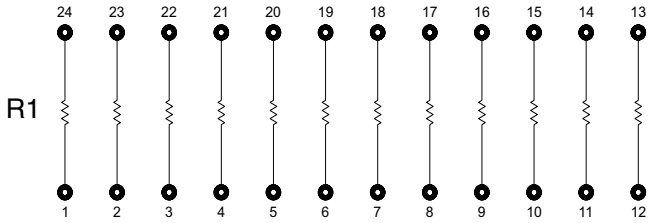
Chip Network Array Series

Physical Data

DQSCX



DQSCA



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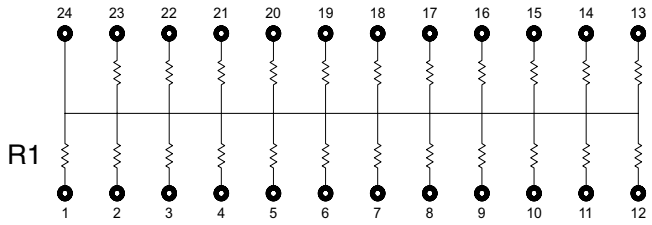

Environmental Data

Test	Method	Max ΔR	Typical ΔR
Thermal Shock	MIL-STD-202 Method 107 Test condition F	±0.1%	±0.02%
High Temperature Exposure	MIL-STD-883 Method 1008 150°C, 1000 hours	±0.1%	±0.05%
Low Temperature Storage	-55°C, 1000 hours	±0.03%	±0.01%
Life	MIL-STD-202 Method 108 70°C, 1000 hours	±0.5%	±0.01%
Life at Elevated Temperature	MIL-STD-202 Method 108 125°C, 1000 hours	±0.5%	±0.05%

Ordering Data

Prefix — WBD DSS8 - B - 01 - 1002 - F - B

Style
DSS4 = 8-pad Network
DSS8 = 6-pad Network
DQSC = 24-pad Network

Schematic and Termination
A = Isolated; B = Bussed

TCR/Inspection Code
Reference TCR/Inspection Code Table

Resistance Code
4-Digit Resistance Code
Ex: 1002 = 10KΩ, 50R1 = 50.1Ω

Absolute Tolerance Code
J = ±5%; G = ±2%; F = ±1%;
D = ±0.5%; C = ±0.25%; B = ±0.1%

Ratio Tolerance Code (optional)
G = ±2%; F = ±1%; D = ±0.5%;
C = ±0.25%; B = ±0.1%; A = 0.05%

Packaging
Standard packaging is 2″ x 2″ chip tray. For additional information or to discuss your specific requirements, please contact our Applications Team using the contact details below.