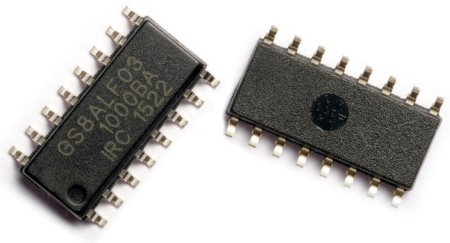
SOIC Thin Film on Ceramic Resistor Networks

SOIC-C Series

OBSOLETE



Features:

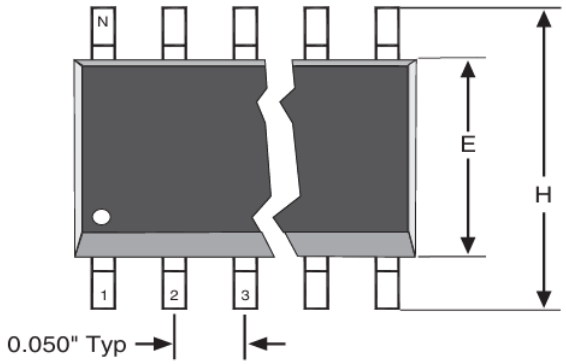
- Precision ratio tolerances to ±0.05%
- Tracking TCR to ±5ppm/°C
- Tested for COTS applications
- Both narrow and wide body versions available
- Standard JEDEC 8, 14, 16 & 20 pin packages
- Ultra-stable TaN resistors on ceramic substrates
- Lower crosstalk than silicon substrate types

All parts are Pb-free and comply with EU Directive 2011/65/EU amended by (EU) 2015/863 (RoHS3)

Electrical Data

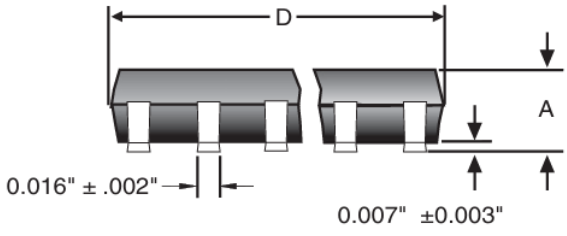
		GS4	GS7	GS8	GL8	GL0
Package style		SOIC-N			SOIC-W	
Number of pins		8	14	16	16	20
Element resistance range	ohms	100R – 200K				
Absolute tolerance	%	0.1, 0.25, 0.5, 1, 2, 5				
Ratio tolerance to R1	%	0.05, 0.1, 0.25, 0.5, 1, 2				
Absolute TCR	ppm/°C	25, 50, 100				
Tracking TCR	ppm/°C	to 5				
Element power rating @70°C	mW	Isolated (A): 100, Bussed (B): 50				
Package power rating @70°C	mW	400	700	800	1200	1500
Rated operating voltage not to exceed √(PxR)	V	100				
Operating temperature	°C	-55 to 125				
Noise	dB	<-25				

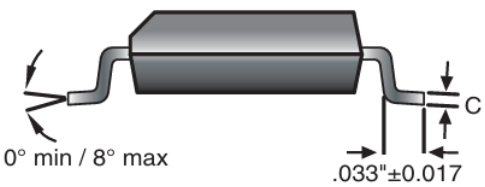
Physical Data



Style	Package	D ±0.004" ±0.1mm	H ±0.008" ±0.2mm	E ±0.004" ±0.1mm	A ±0.004" ±0.1mm	C
GS4	SOIC-N-8	0.193" 4.9mm	0.236" 5.99mm	0.153" 3.89mm	0.064" 1.63mm	0.0075" ±0.01 0.19mm ±0.25
GS7	SOIC-N-14	0.341" 8.66mm				
GS8	SOIC-N-16	0.39" 9.91mm				
GL8	SOIC-W-16	0.402" 10.2mm	0.406" 10.3mm	0.295" 7.49mm	0.1" 2.54mm	0.011" ±0.002 0.28mm ±0.05
GL0	SOIC-W-20	0.502" 12.8mm				

Note 1: All dimensions exclude mold flash and end flash which shall not exceed 0.006" (0.15mm) per side.
Note 2: Lead coplanarity 0.004" (0.1mm) max.





Marking

The product is marked with style, schematic code, TCR code, value and tolerance code.

General Note
TT Electronics reserves the right to make changes in product specification without notice or liability.
All information is subject to TT Electronics' own data and is considered accurate at time of going to print.

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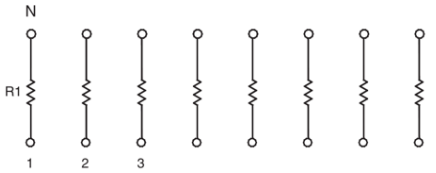
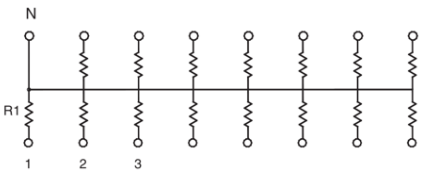
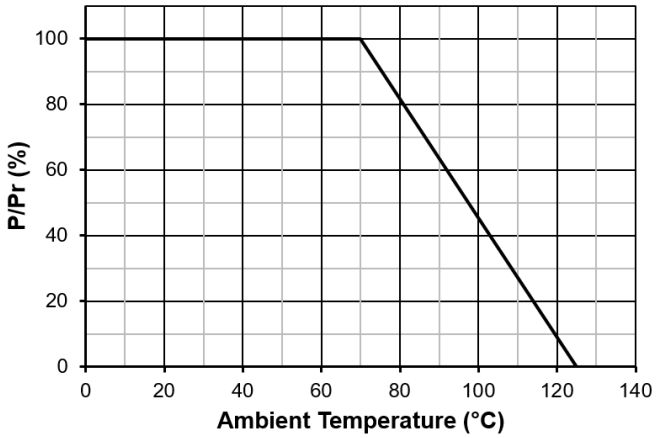
Schematic Data

	Isolated (A)		Bussed (B)	
				
Style	**Number of Pins (N)**	**Number of Elements**	**Number of Pins (N)**	**Number of Elements**
GS4	8	4	8	7
GS7	14	7	14	13
GS8, GL8	16	8	16	15
GL0	20	10	20	19

Performance Data

Test per MIL-PRF-83401	±ΔR/R%	
	Typical	Maximum
Thermal shock	0.02	0.1
Power conditioning	0.03	0.1
High temperature exposure	0.03	0.05
Short-time overload	0.02	0.05
Low temperature storage	0.03	0.05
Life	0.05	0.1

Temperature Derating



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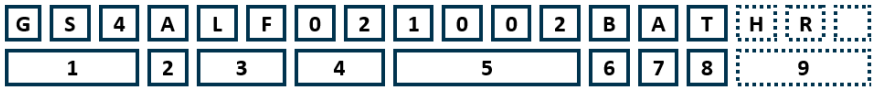
Ordering Procedure

Example: GS4ALF021002BATHR (8-pin narrow SOIC, isolated elements, Pb-free, 50ppm/°C, 10 kilohms, absolute tolerance ±0.1%, ratio tolerance ±0.05%, tube packed, variant HR)



1 Style	2 Schematic	3 Termination	4 Absolute TCR	5 Value	6 Absolute Tolerance	7 Ratio Tolerance	8 Packing	9 Variant
GS4	A = Isolated	LF = Pb-free (100%Sn)	03 = ±25ppm/°C	3 digits + multiplier R = ohms for values <100 ohms	B = ±0.1%	A = ±0.05%	T = Tube	Omit for standard
GS7	B = Bussed		02 = ±50ppm/°C		C = ±0.25%	B = ±0.1%	R = Reel	HR = High reliability screened (50 cycles thermal shock)
GS8			01 = ±100ppm/°C		D = ±0.5%	C = ±0.25%		
GL8					F = ±1%	D = ±0.5%		
GL0					G = ±2%	F = ±1%		
					J = ±5%	G = ±2%		

Note 1: Legacy part numbers may have the Variant code placed after the Schematic code, e.g. **GS4AHRLF021002BAT**.
Note 2: Legacy part numbers may be prefixed by **GUL-**, e.g. **GUL-GS4ALF021002BATHR**.

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