TT Electronics

Specification Demystification:

Understanding Power Supply Hold-Up Time

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Introduction

While many of the developed world's power grids are robust and mature systems, they are not perfect. The mains voltage (available from the outlets in homes, offices, hospitals and other facilities), supplying power to the electrical devices we use every day, is vulnerable to a number of complications. The AC/DC converters we employ to turn that mains voltage into something our devices can actually use should be designed with these complications in mind and should offer some level of protection against them. How well a given power converter responds to one such complication: momentary dropouts, can be gleaned from its specified hold-up time. This month's technical bulletin will provide a comprehensive overview of power supply hold-up time: why it matters, how it is determined, and how it is measured.

> Hold-up time is a fundamental performance metric for any power supply.

WHAT IS HOLD-UP TIME?

When an AC drop-out or interruption occurs, Hold-Up time is the time between the discontinuity in the AC voltage waveform and the corresponding reduction in DC output voltage to the lower limit of its specified regulation. This assessment is made under full rated load conditions. Simply put, Hold-Up time is how long the PSU operates within specification after its source has been removed. Power converters designed for use in commercial, industrial, or medical applications typically exhibit hold-up times on the order of tens of milliseconds. Hold-Up time (t_{HU}) is depicted in Figure 1, the dotted black line in the DC plot represents the lower limit of the specified DC regulation.

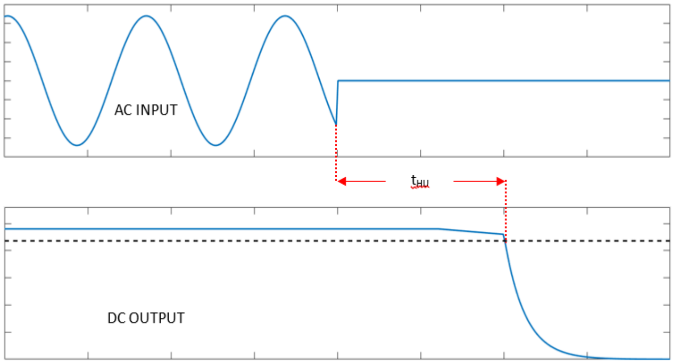


Figure 1

Graphic Decipiction of Hold-Up Time

WHY HOLD-UP TIME MATTERS

Downstream Device Resets:

This seemingly brief period of time between the respective collapses of the AC and DC voltages holds good deal of significance. This delay is the maximum duration for which your downstream DC device would remain functional (assuming it does not have a battery back up) during a brief mains interruption.

That is, for any interruption of a duration less than t_{HU}, downstream devices would essentially be none the wiser. Consider the difference in behavior of two power supplies fed from the same outlet in the event of a 10ms AC drop out. Power Supply A has a specified hold-up time of 8.3ms while Power Supply B has a specified hold-up time of 12ms. Their respective responses to the drop out are shown in Figure 2.

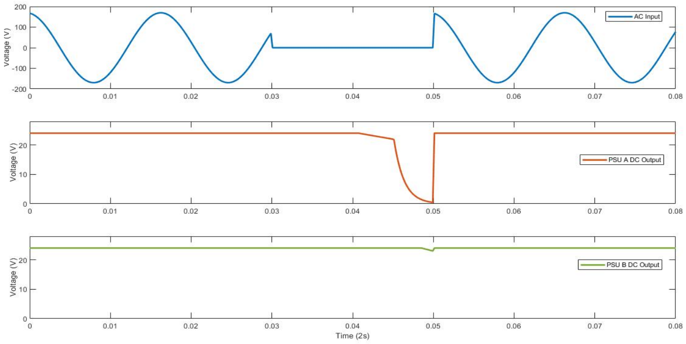


Figure 2

Example: Impact of Hold-Up Time

IEC 61000-4-11:

The ability to, or more specifically the degree to which, a given power supply passes IEC 61000-4-11 (Voltage Dips and Interruptions Immunity) testing is also directly dependent upon its hold-up capabilities. 61000-4-11 specifies input voltage reduction ratios and a respective number AC cycles for which the PSU must be subjected to that reduction. This test is most commonly conducted under European line voltages towards CE mark requirements, and so the line frequency for the test is typically 50Hz. 50Hz corresponds to a single cycle duration, or period of 20ms and so a power supply with a specified hold up time of 10ms, should be expected to pass the well known >95% reduction, ½ cycle test under criteria “A”, signifying no performance degradation, where as one with less then 10ms of hold up might only achieve criteria “B”. A similar analysis can be carried out for the other tests in the IEC 61000-4-11 standard.

Power Fail Detection:

Some power supplies have built in power fail alarm signals that indicate the occurrence of an AC drop-out, in advance of the collapse of the DC rail. This signal is often used to trigger a proper shut-down sequence for any downstream processors or other devices that may be subject to corruption in the event of a sudden loss of power. The power supply's hold-up capability plays a major role in this feature, and determines (in part) how long a downstream device will have to complete its shutdown sequence before DC power is lost.

DETERMINATION OF HOLD-UP TIME

A power supply's hold-up capability is almost entirely attributable to two parameters; the nominal voltage of the primary side high-voltage (HV) rail, and the bulk capacitance across that rail. These two figures can be used to calculate the energy stored on the primary side of the converter according to [1]

$$E_P = \frac{C_{HV}V_{HV}^2}{2} \qquad [1]$$

Where E_P is the energy stored on the primary in Joules, C_{HV} is the bulk capacitance across the HV rail in Farads, and V_{HV} is the nominal voltage on the HV rail in Volts.

As a starting point toward the determination of a converter's hold-up capability, realize that once the AC energy source has been removed or turned off, this energy store (E_P) is all that remains to be converted.

> ASIDE: Note that energy stored on the secondary or on an auxiliary rail is negligible in hold-up determination for all but the smallest of converters (and even then it does not contribute much). The secondary is almost always an SELV network (<60VDC), and voltage is of course the dominant term in the energy equation as it is second order. The effect of this dominance will become more clear when a typical AC/DC converter shutdown sequence is presented later in this discussion.

A quick energy-power calculation [2] would tell us that the hold up time cannot exceed the ratio of the primary energy store to the rated output power. But in reality, there is a bit more to the determination than this simple ratio.

$$t_{HU_{MAX}} \leq \frac{E_P}{P_{Rated}} \tag{2}$$

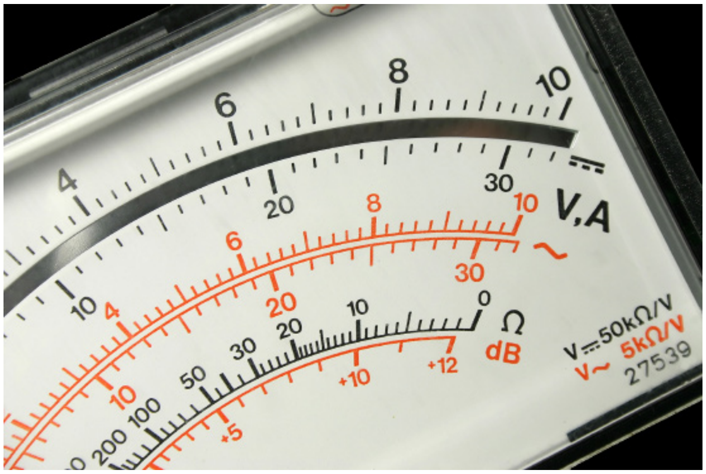
The first deviation from this simple ratio comes from the understanding that almost all of the power converters losses are downstream of the HV rail. Consider the fact that conduction losses on the primary are almost negligible compared to those on the secondary due to the second order influence of current, currents being much lower on the primary. Further, all switching losses and most losses associated with magnetics occur just downstream of the HV rail. Accordingly, for the purposes of hold up determination, we can assume [3].

$$P_{d_{HV}} = \frac{P_{rated}}{\eta_{FL}} \tag{3}$$

Where P_{dHV} is the power drawn off the HV rail in Watts, and η_{FL} is the nominal full load efficiency of the converter. We then refine [2] in [4]

$$t_{HU_{MAX}} \leq \frac{E_P}{P_{d_{HV}}} \leq \frac{E_P}{P_{Rated}} \tag{4}$$

Lastly, recognize that the networks that control and regulate the converter require energy to operate. As is true for any active circuit, there is a supply voltage below which the circuit will cease to operate in the intended manner. The control circuits on most power converters run on a supply voltage of somewhere between 10VDC and 20VDC, but this can really vary quite a bit from design to design. This low voltage rail is usually developed from an auxiliary winding on the main transformer, rectified and filtered, and its regulation tracks that of the main output around which the feedback loop is closed.



If this voltage drops below some value, the control network will cease to function.

Now is a good time to take a look at a typical shutdown sequence, and exactly what happens after the AC supply is removed. This process is exemplified in Figure 3 which shows the change in DC output voltage of a typical switching power supply as it shuts down following a source interruption and highlights critical events. Each section has been graphically exaggerated for demonstrative purposes.

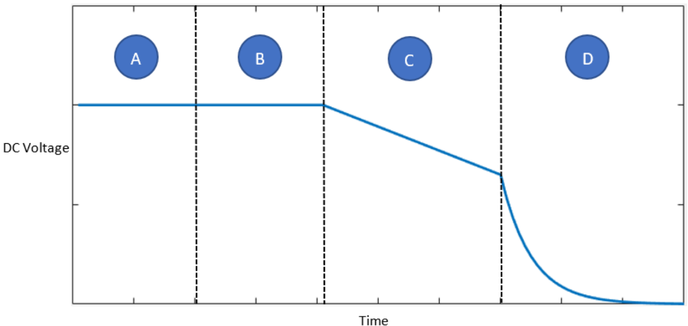


Figure 3
Typical SMPS Shutdown Sequence

A: Pre-Interruption

The PSU is functioning under normal operating conditions, DC output voltage is constant.

B: Immediately following interruption

The AC source has been disconnected, and there is no longer an external source of energy. The PSU begins depleting the energy stored in the electric field within the bulk capacitance across the HV rail. As the energy stored in this field is consumed by the load and the conversion losses, the voltage across the rail (V_{HV}) begins to decrease according to [1]. In response, the converter adjusts *g* to maintain the nominal output voltage (V_{OUT}), where *g* is a topology dependent function of switching frequency (f_{sw}), transformer turns ratio (n), and duty cycle (D) that relates V_{HV} to V_{OUT} according to [5]

$$V_{OUT} = g(f_{sw}, n, D) \cdot V_H \qquad [5]$$

For any given topology, there exists a maximum value that *g* can assume. Once *g* has reached its maximum value, as determined by constraints of the conversion topology, the shutdown sequence continues into section C.

C: V_{OUT} and V_{AUX} decay with V_{HV}

The converter has adjusted its duty cycle and/or switching frequency to the limits of the topology, and *g* assumes a fixed maximum value. V_{OUT} and V_{AUX} are now forced to decay with V_{HV} as E_p continues to be consumed by the load and conversion losses. The shape of the curve in this section is dependent upon the nature of the load, here we approximate the curve as a straight line. Hold-Up time is generally assessed with a resistive load, such that the voltage would actually decay exponentially, as it does in section D, but this period is typically very short lived, and the time constant of the decay is so much greater than that seen in section D, that in our exaggerated shutdown sequence plot, a straight line is a reasonable visual approximation.

This decay continues until $V_{AUX} < V_{CC\ MIN}$, where $V_{CC\ MIN}$ is the lowest DC supply voltage that will allow the PWM control circuit to continue to trigger gate pulses to the primary side switch(s). At that time, energy transfer from primary to secondary ceases.

D: Depletion of energy in secondary filter elements

After energy transfer stops, the converter is effectively in shutdown. The load will now consume what ever energy is stored in the secondary side filter elements, and V_{OUT} will decay at a much faster rate as a result of the relatively small capacitance on this side of the converter.

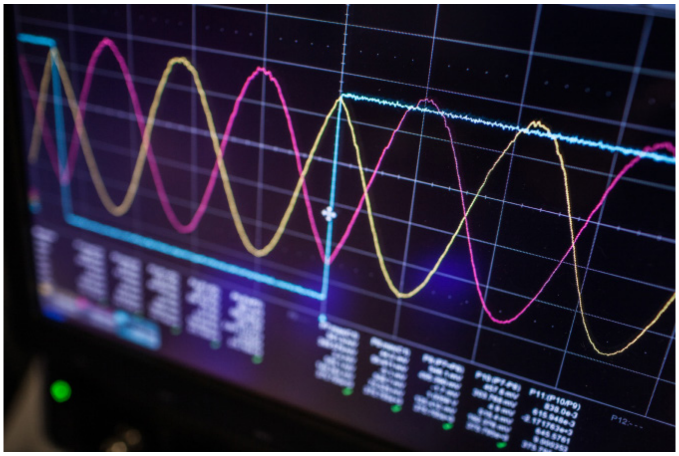
The exact V_{AUX} voltage at which the converter transitions into shut down (depicted above as the transition between C and D) will vary from device to device. That minimum V_{AUX} voltage, call it $V_{AUX_{MIN}}$, corresponds directly to a particular V_{HV} voltage, $V_{HV_{MIN}}$ which in turn corresponds directly to a given energy storage level in the primary bulk capacitance, $E_{P_{MIN}}$, according to [1]. With this, we further refine [4] in [6], which is an approximate model for the hold-up time of a typical switch mode power converter.

$$t_{HU} \approx \frac{E_P - E_{P_{MIN}}}{P_{d_{HV}}} = \frac{C_{HV}\,\eta_{FL}}{2\,P_{RATED}}\left(V_{HV}^2 - {V_{HV}}_{MIN}^{\,2}\right) \leq {t_{HU}}_{MAX} \leq \frac{E_P}{P_{d_{HV}}} \leq \frac{E_P}{P_{Rated}} \quad [6]$$

The inequalities have been left in place to provide a means for quickly assessing a maximum bound on a given converters hold-up time by inspection alone. That is, one can read the rated voltage and capacitance right off the primary side bulk capacitance and determine the absolute maximum hold-up time that could be exhibited. The estimate could then be further refined (in increasing order of difficulty of ascertainment) with knowledge of the converters efficiency, a measurement of the HV rails nominal voltage (as opposed to the capacitors rated voltage), and finally knowledge of $V_{AUX_{MIN}}$.

MEASURING HOLD-UP TIME

Measuring hold-up time is a particularly simple exercise. Ideally, one would employ a two-channel oscilloscope with at least one channel being fed by a differential probe (there are ways around this), an adjustable DC load, and in the case of a non-power factor corrected converter (sub-75W), an adjustable AC source may also be desired.



If the design is power factor corrected, which is typically the case for any converter with a throughput of at least 75W, then V_{HV} is regulated. Accordingly, the AC RMS input voltage will have almost no impact on the hold-up time. For non-power factor corrected converter, the AC input voltage has a profound impact on hold up time, as it is directly related to V_{HV}. This relationship is detailed in [7].

$$V_{HV} = \sqrt{2}V_{IN_{RMS}} - 2V_{FWD} - V_{CON} \approx \sqrt{2}V_{IN_{RMS}} \quad [7]$$

Where V_{FWD} is the forward voltage of a single diode in the 60Hz rectifier and V_{CON} represents any conduction losses in AC cabling, and primary side EMC filtering. Both are essentially negligible for this excersize.

Per [7] and [6], one can measure the minimum hold-up time for a non-power factor corrected converter by running the test at the minimum specified input voltage.

To perform the measurement, one should place the differential probe across Line and Neutral at the input to the power converter, and the second probe across the DC output. The differential probe is used because the primary side and secondary side of the isolated converter have different returns/references which are likely held at a significant potential from each other. Using two standard probes, which would each share a common reference, creates a short circuit across the isolated converter via the oscilloscope, and will usually cause catastrophic damage. If a differential probe is not available, another option is to monitor either Line or Neutral referenced to the secondary return. This practice can of course corrupt the observed value of the measurement taken on the primary side, but for hold-up determination the exact value of the incoming AC voltage at any given time is not of importance. Rather, a discontinuity in the sinusoidal waveform is all that needs to be observed for hold-up determination.

With the probes properly connected, and the device powered on, one can observe the nominal DC output voltage and a sinusoidal waveform equal to or representative of the incoming AC on separate traces on the oscilloscope. The scope should be configured to trigger on a falling edge on the channel measuring the DC, at a threshold equal to the minimum specified allowable output voltage. For instance, if the PSU is specified as having an output of 24V ± 5%, the trigger threshold should be set to 22.8V. Considering that hold-up times are generally on the order of a few 10's of milliseconds, the horizontal time scale should be adjusted to 5 or 10ms per division and can be refined as necessary in subsequent measurements.

At this time, the resistive DC load can be adjusted to draw the maximum rated current from the power supply. Recall that the observed hold up is inversely proportional to the power consumed by the load. Next, a single sequence acquisition should be initiated, and the AC source should be indefinitely interrupted. Cursor tools can then be used to measure the time delta between the trigger event and the AC discontinuity as exemplified in Figure 4.

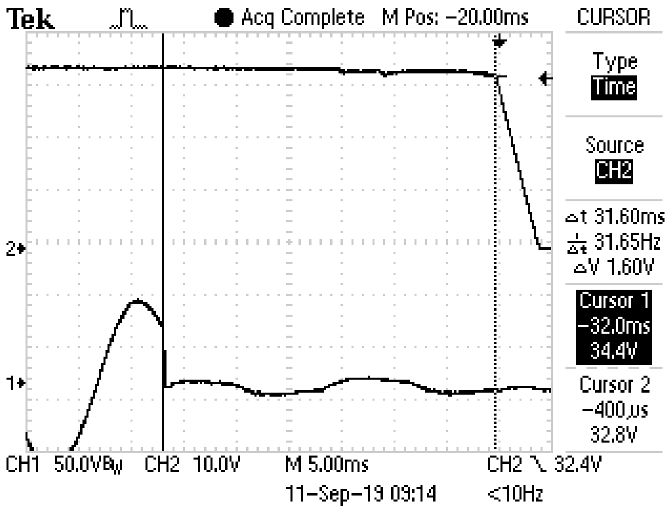


Figure 4

Single Sequence Acquisition of Hold-Up Time

Note that in Figure 4, we have used the secondary return as the reference for the primary side measurement, effectively mitigating the need for a differential probe. This results in an inaccurate display of the true AC voltage across the observation period, but notice that the discontinuity is still exceptionally clear. The hold-up time in the above example is 32ms (note the 400µs delta between curser two and the true trigger point due to cursor resolution issues at this time scale).

CONCLUSION

Hold-up time is a fundamental performance metric for any power supply. To effectively compare the hold-up performance of different solutions, or to analyze the impact of the hold-up time on the overall performance of the system, it is important to understand how the parameter is defined, determined, and measured. To learn more about how hold-up time may play a role in your next design, reach out to a member of our team today.